

**CLAIMS**

Please cancel claims 1-14 without prejudice.

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)

Please add new claims 15-21:

15. (New) A method of producing a semiconductor device having metal wiring, comprising steps of:

forming metal wiring containing an additive on a first insulation film formed in a semiconductor substrate;

forming on said metal wiring a barrier layer for preventing diffusion of constituting elements of said metal wiring, said step of forming the barrier layer further comprising the step of performing an electroless plating step, said electroless plating step comprising a catalyst plating step and a washing step;

forming a second insulation film on said barrier layer;

wherein said additive is an element to reduce corrosion of said metal wiring at the time of forming said barrier layer.

16. (New) A method of producing a semiconductor device as set forth in claim 15, wherein said additive includes an element having less ionization tendency than a catalyst substance to be plated in said catalyst plating process.

17. (New) A method of producing a semiconductor device as set forth in claim 15, wherein:

the step of forming said metal wiring includes a step of forming a seed layer of the metal wiring and a step of forming the metal wiring integrally with the seed layer; and

said additive is mixed in said seed layer for the formation.

18. (New) A method of producing a semiconductor device as set forth in claim 15, wherein:

the step of forming said metal wiring includes a step of forming a seed layer of the metal wiring and a step of forming the metal wiring integrally with the seed layer; and

said additive is stacked in said seed layer for the formation.

19. (New) A method of producing a semiconductor device as set forth in claim 15, wherein a step of performing heat treatment so that said additive segregates on a grain boundary of said metal wiring is further included after the step of forming said metal wiring.

20. (New) A method of producing a semiconductor device as set forth in claim 15 wherein:

the step of forming said metal wiring includes a step of forming a seed layer of the metal wiring and a step of forming the metal wiring integrally with the seed layer; and

said additive is mixed in said metal wiring in the step of forming the metal wiring integrally with the seed layer.

21. (New) A method of producing a semiconductor device as set forth in claim 16, wherein:

the catalyst substance to be plated in said catalyst plating step is palladium (Pd); and

the element having the less ionization tendency than the catalyst substance to be plated in said catalyst plating step contains any one of iridium (Ir), platinum (Pt) and gold (Au).